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| 09/866,092 | 05/23/2001 | Mark Thomas McCormack | 6136/54242 (25916-217) | 5484 |

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| EXAMINER | |
|---|---|
| LEE, EUGENE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 07/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/866,092 | MCCORMACK ET AL. | |
| | Examiner | Art Unit | |
| | Eugene Lee | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *17-24,26-34 and 36-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-24,26-34,36-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

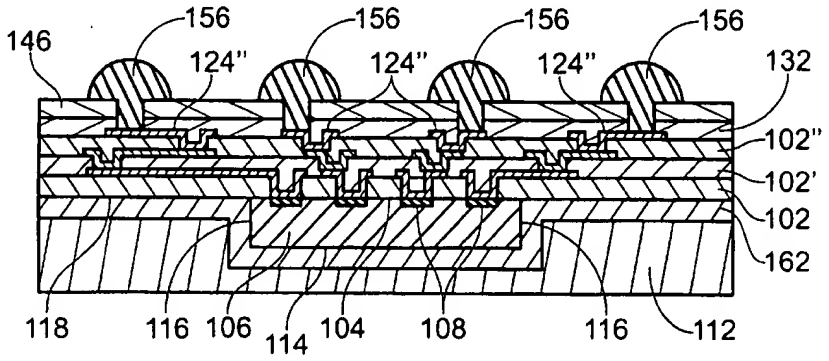
### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. 6,154,366 in view of Saito et al. 5,049,980 in view of Cole, Jr. et al. 5,073,814. Ma discloses (see, for example, Fig. 2j) a package (multi-layer printed circuit board) comprising an encapsulation material (circuit board substrate) 112 having a first substrate surface and a second substrate surface, die (first integrated electronic component) 106, cavity, flex component (first dielectric layer) 102, conductive trace (metallic layer) 124, electrically conductive first via, element (second dielectric layer) 102', and electrically conductive second via.

Fig. 2j




Ma does not disclose the circuit board substrate being polymeric. However, Saito discloses (see, for example, FIG. 5) an electronic circuit device comprising a semiconductor element 2, and resin substrate (circuit board substrate) 1. In column 2, lines 42-46, Saito discloses the resin

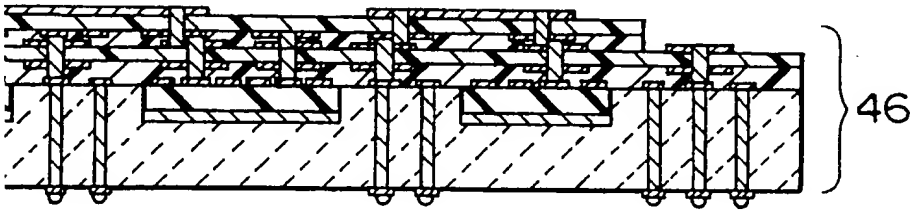
substrate may be a polycarbonate resin, which is polymeric. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the circuit board substrate being polymeric in order to have a material that adequately supports a die, and any overlying layers wherein the material is not prone to cracking.

Ma in view of Saito does not disclose a second electrically conductive via extending at one location. However, Cole discloses (see, for example, FIG. 1) a structure 10 comprising a metal (second electrically conductive via) 30 in via holes 28. The metal extends at one location through alternating sublayers of dielectric material 24, 26. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second electrically conductive via extending at one location in order to lessen manufacture time by laying down one layer instead of multiple layers.

Regarding claims 38, and 39, these claims contain product-by-process limitations (i.e. is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board (claim 38), and at a temperature of greater than about 600 C (claim 39)) that do not structurally differentiate the applicant's claimed structure from Ma in view of Saito.

3. Claims 17, 18, 20 thru 23, 27, 30, 36, 38 thru 41, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. 5,565,706 in view of Saito et al. 5,049,980 in view of Cole, Jr. et al. 5,073,814. Miura discloses (see, for example, FIG. 6) a multi-layer package board (multi-layer printed circuit board) comprising a package board (circuit board substrate) 46; ceramic substrate (core) 45 having a first substrate surface and a second substrate surface; LSI (first integrated electronic component) 35, spot facing portions (cavity) 37, adhesive sheet (first

dielectric layer) 11, copper wiring (metallic layer) 9a, via (electrically conductive first via) 17, insulating layer (second dielectric layer) 9c, and via (electrically conductive second via) 16.




Miura does not disclose the circuit board substrate being polymeric. However, Saito discloses (see, for example, FIG. 5) an electronic circuit device comprising a semiconductor element 2, and resin substrate (circuit board substrate) 1. In column 2, lines 42-46, Saito discloses the resin substrate may be a polycarbonate resin, which is polymeric. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the circuit board substrate being polymeric in order to have a material that adequately supports a die, and any overlying layers wherein the material is not prone to cracking.

Miura in view of Saito does not disclose a second electrically conductive via extending at one location. However, Cole discloses (see, for example, FIG. 1) a structure 10 comprising a metal (second electrically conductive via) 30 in via holes 28. The metal extends at one location through alternating sublayers of dielectric material 24, 26. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second electrically conductive via extending at one location in order to lessen manufacture time by laying down one layer instead of multiple layers.

Regarding claim 18, see figures wherein Miura discloses external output terminals (first metallic layer) 8 and external output terminals (second metallic layer) 28.

Regarding claim 27, see figures wherein Miura discloses external output terminals (conductive pad) 8 on top of the LSI 35.

Regarding claim 30, see FIG. 6 wherein Miura discloses one of the vias (at least one metal-lined via) 16 attached to LSI 33.

Regarding claim 36, see, for example, column 8, lines 25-28 wherein Miura discloses a capacitor.

Regarding claims 38, and 39, these claims contain product-by-process limitations (i.e. is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board (claim 38), and at a temperature of greater than about 600 C (claim 39)) that do not structurally differentiate the applicant's claimed structure from Ma in view of Saito in view of Cole, Jr.

4. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. '706 in view of Saito et al. '980 in view of Cole, Jr. et al. '814 as applied to claims 17, 18, 20-23, 27, 30, 36, 38-41, 43, and 44 above, and further in view of Desai 5,739,188. Miura in view of Saito in view of Cole does not disclose the multi-layer core substrate comprising at least two polymeric layers. However, Desai discloses (see, for example, column 3, lines 26-30) a multi layered product wherein the product comprises a substrate layer/cap layer (two polymeric layers). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the multi-layer core substrate comprising at least two polymeric layers in order to protect the substrate.

5. Claims 24, 26, 28, 29, 31, 32, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. '706 in view of Saito et al. '980 in view of Cole, Jr. et al. '814 as applied to claims 17, 18, 20-23, 27, 30, 36, 38-41, 43, and 44 above, and further in view of Marcinkiewicz et al. 5,241,456. Miura in view of Saito in view of Cole does not disclose said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component disposed in said cavity. However, Marcinkiewicz discloses (see, for example, FIG. 1) a structure 10 comprising a substrate 12, and chip (second integrated electronic component) 36. Having the chip in the same substrate creates a multichip device that saves space and provides interconnection between two chips. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said exposed portion of said second substrate surface including a cavity additionally comprising a second integrated electronic component disposed in said cavity in order to create a multichip device that saves space and provides interconnection between two chips.

Regarding claim 28, see, for example, FIG. 1 wherein Marcinkiewicz discloses contact pad (conductive pad) 38.

Regarding claim 29, see, for example, FIG. 1 wherein Miura discloses contact pad (conductive pad) 8 on top of the LSI 35.

Regarding claim 44, Miura in view of Saito does not disclose a third dielectric layer disposed on said second side of said substrate. However, Marcinkiewicz discloses (see, for example, FIG. 1) a substrate 12, and dielectric layer (third dielectric layer) 52. The dielectric layer protects the bottom surface of the substrate. Therefore, it would have been obvious to one

of ordinary skill in the art at the time of invention to have a third dielectric layer disposed on said second side of said substrate in order to protect the bottom of the substate.

6. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. '706 in view of Saito et al. '980 in view of Cole, Jr. et al. '814 as applied to claims 17, 18, 20-23, 27, 30, 36, 38-41, 43, and 44 above, and further in view of Ma et al. 6,154,366. Miura in view of Saito in view of Cole does not disclose additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer. However, Ma discloses (see, for example, FIG. 1d) a package comprising a die 106 and multiple conductive traces (at least one metal-lined via) 124. The multiple conductive traces transmit signals to the die. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have additionally at least one metal-lined via extending through said metallic layer and through said first dielectric layer in order to transmit more signals to the integrated electronic component.

7. Claims 37, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. '706 in view of Saito et al. '980 in view of Cole, Jr. et al. '814 as applied to claims 17, 18, 20-23, 27, 30, 36, 38-41, 43, and 44 above, and further in view of Miyazawa et al. 5,953,619. Miura in view of Saito in view of Cole does not disclose said capacitor comprising a perovskite capacitance material. However, Miyazawa discloses (see, for example, column 1, lines 27-35) that a perovskite crystal structure has a high dielectric constant. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said capacitor

comprising a perovskite capacitance material in order to have a higher dielectric constant in the same area.

***Response to Arguments***

8. Applicant's arguments with respect to claims 17-24, 26-34, and 36-44 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the applicant's argument on page 1, second paragraph that Ma does not show a cavity formed in a core substrate in which a prefabricated component is mounted, this argument is not persuasive. The claim only states structurally a core wherein the core is polymeric. Further, a preamble (i.e. multi-layered printed circuit board) is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951). On page 10 of the specification, the applicant states that the core need only be made of polymeric compounds, etc., which Ma (or Miura) in view of Saito in of Cole, Jr. structurally discloses.

Regarding the applicant's argument on page 11, third and fourth paragraphs that there is no reason shown why someone skilled in the art would be motivated to replace the ceramic substrate of Mirua with a polymeric substrate, this argument is not persuasive. There is no requirement that a motivation to make a modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971) references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures.

In re Bozek, 163 USPQ 545 (CCPA 1969). In this case, resin (as disclosed by Saito) is generally known as a more flexible, softer material that ceramic, and, therefore, less likely to break. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use resin instead of ceramic in order to form the chip on a material less likely to break.

### *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eugene Lee
June 26, 2006

EUGENE LEE
PRIMARY EXAMINER